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APPLICATION NUMBER: *60/370,071*
FILING DATE: *April 04, 2002*
RELATED PCT APPLICATION NUMBER: *PCT/US03/10278*

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
John Barrett	George	Carmel, Indiana
Kevin Michael	Williams	Indianapolis, Indiana

☐ *Additional inventors are being named on the _____ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

POWER SUPPLY PROTECTION ARRANGEMENT

CORRESPONDENCE ADDRESS

Direct all correspondence to:

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☒ Firm *or* Individual Name	THOMSON MULTIMEDIA LICENSING INC.				
Address	PATENT OPERATIONS				
Address	P. O. BOX 5312				
City	PRINCETON	State	NJ	ZIP	08543-5312
Country	USA	Telephone	609/734-9751	Fax	609-734-9700

ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* [8] ☐ CD(s), Number [ ]

☒ Drawing(s) *Number of Sheets* [3] ☐ Other (specify) [ ]

☐ Application Data Sheet. See 37 CFR 1.76

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☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: [07-0832]

FILING FEE AMOUNT ($) [160]

☐ Payment by credit card. Form PTO-2038 is attached.

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____.

Respectfully submitted,

SIGNATURE [signature]

Date [4/4/02]

TYPED or PRINTED NAME Sammy S. Henig

REGISTRATION NO. *(if appropriate)* [30,263]

TELEPHONE PU020090

Docket Number: [PU020090]

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Complete if Known	
Application Number	
Filing Date	Herewith
First Named Inventor	John Barrett George
Examiner Name	
Group / Art Unit	
Attorney Docket No.	PU020090

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	160.00

SUBTOTAL (1) ($) 160.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20 ** =		X		=	
Independent Claims		-3 ** =		X		=	
Multiple Dependent				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17 (q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY			Complete (if applicable)		
Name (Print/Type)	Sammy S. Henig	Registration No. Attorney/Agent)	30,263	Telephone	609/734-9751
Signature	[signature]			Date	4/4/02

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POWER SUPPLY PROTECTION ARRANGEMENT

Background of the Invention

The invention relates to a power supply protection arrangement of a video display apparatus, for example, a projection television (TV) receiver.

The displayed image in, for example, a direct view TV receiver or in a projection TV receiver having a cathode ray tube (CRT), may suffer from electron beam landing location errors such as geometrical and convergence errors. It is known to correct such errors for a CRT using a dynamic convergence arrangement. The amount of correction may vary dynamically in a given deflection cycle, in accordance with the location of the beam on the display screen.

In one prior art arrangement, to minimize manufacturing costs of a direct view TV receiver model and a projection TV receiver model, both models shared the same chassis. The main deflection circuits were common. Direct view models used about 90% of the chassis. For economic reasons the main chassis power supply was sized for the direct view model and a projection convergence power supply was added on for a projection TV receiver model .

When, as a result of a fault, a supply current exceeds a predetermined value, a threshold level of a protection detector is exceeded and causes the dedicated convergence switch mode power supply to shut down. Trouble shooting convenience requires that the TV receiver show a picture when the convergence circuits have a fault. Thus, the rest of the TV receiver circuits including the deflection circuits remain energized and operational. The convergence dedicated switch mode supply remains turned off until the projection TV receiver is turned off and then on, again, by a user.

In carrying out an inventive feature, a common switch mode power supply energizes the convergence circuits and the rest of the TV receiver circuits. Instead of using the prior art separate power supplies solution, a fast acting latching power supply voltage disconnect arrangement for the convergence circuits is utilized. Such arrangement provides a cost advantage.

FIGURE 1 illustrates an example of a prior art power amplifier that drives the convergence winding in a CRT of the projection video display, shown in FIGURE 3 of United States Patent No. 4,961,032 in the name of Rodriguez-Cavazos, entitled, Dual Power Source Output Amplifier (the Rodriguez-Cavazos patent). The symbols and reference numerals in FIGURE 1 are the same as in FIGURE 3 of the Rodriguez-Cavazos patent except that a prime sign (') is appended to each.

In FIGURE 1, an amplifier 50' comprises a differential amplifier 12', a buffer 14' and one output stage 16'. The differential amplifier 12' is formed by transistors Q1' and Q2'. An input waveform signal V_{IN}' is connected to the base of transistor Q1'. The collector of transistor Q1' is connected to a high voltage supply source of positive polarity voltage $+V_H$'. The emitters of transistors Q1' and Q2' are connected together, and through a resistor R1', to a negative high supply voltage $-V_H$'. A parallel combination of sense resistors R21' and R22' are connected to a deflection coil 24' of a yoke Y1' and the base of transistor Q2', for developing the sense voltage V_S. A transistor Q11' converts the output current at the collector of transistor Q2' into an output voltage across a load resistor R18'. Diodes D8', D9', D10' and D11' establish a biasing voltage for the buffer stage 14', which includes transistors Q9' and Q10'. The emitters of transistors Q9' and Q10' of the buffer stage drive the bases of transistors Q4' and Q5', respectively, through resistors R13' and R14', respectively. Transistors Q4' and Q5' form class B output stage 16'. The emitters of transistors Q4' and Q5' are connected to resistors R7' and R8', respectively. The output voltage signal of the amplifier is generated at the junction of resistors R7' and R8', which is connected to the coil 24' of convergence yoke Y1'.

Output stage 16' provides high current. It needs to provide a high voltage drive, during horizontal retrace, and a low voltage drive, outside horizontal retrace. Output stage 16' compares dynamically varying input signal V_{IN}' to sense voltage V_S developed across current sense resistors R21' and R22' that are coupled in series with the convergence winding. Output stage 16' generates the necessary current to minimize any difference between the varying input signal V_{IN}' and sense voltage V_S'.

If positive polarity voltage $+V_H$' is turned off and, simultaneously, negative voltage supply $-V_H$' is turned on, during a power-up or start-up interval, transistors Q10' and Q5' will turn on at the limit. Consequently, a current I_{Y1}' in convergence yoke Y1' having an excessive magnitude flows also in sense resistors R21' and R22' that could damage them. Even a short term overstress may cause an unacceptable sense resistor value change. A sense resistor value change causes an uncompensated change in convergence correction gain that distorts the picture.

In a power supply embodying an inventive feature, a positive polarity voltage that is analogous to voltage $+V_H$' is turned on prior to turning on of negative voltage supply that is analogous to voltage $-V_H$', during the power-up or start-up interval. Furthermore, a power supply circuit breaking protection is employed that prevents excessive current in the sense resistors, as a result of a failure in the feedback loop.

Brief Description of the Drawings

FIGURE 1 illustrates a prior art power amplifier that drives a convergence winding of a projection video display;

FIGURE 2a illustrates a prior art deflection system of a projection television receiver; and

FIGURE 2b illustrates a power supply having a protection arrangement, embodying an inventive feature, for the power amplifier of FIGURE 2a.

Description of the Preferred Embodiments

FIGURE 2a illustrates, in block diagram form, a conventional deflection system 100 of a projection television receiver. Deflection system 100 provides dynamic convergence. Three cathode ray tubes (CRT's), R, G and B produce electron beams that form a combined image 800 on a screen 700. The deflection field in each CRT is controlled in a similar way. For example, CRT G is equipped with a main horizontal deflection coil driven by a horizontal deflection output stage 600 and with a main vertical deflection coil driven by a vertical deflection amplifier 650, conventionally constructed. CRT G is also depicted with an auxiliary horizontal convergence coil 615 driven by a horizontal convergence amplifier 610 and with an auxiliary vertical convergence coil 665 driven by a vertical convergence amplifier stage or amplifier 660. Amplifier 660 is energized by a positive supply voltage OUT+ and by a negative supply voltage OUT-. Correction data stored in a memory, not shown, are applied via a digital-to-analog (D/A) converter 312 and power amplifier 660 to auxiliary vertical convergence coil 665.

Amplifier 660 may have a similar topology as the amplifier described in the Rodriguez-Cavazos patent, shown in FIGURE 1. For example, voltage OUT+ of FIGURE 2a will be applied to the amplifier of FIGURE 1 instead of voltage $+V_H$' and voltage OUT- of FIGURE 2a will be applied to the amplifier of FIGURE 1 instead of voltage $-V_H$'.

FIGURE 2b illustrates, in details, a power supply protection arrangement 200, embodying an inventive feature. Similar symbols and numerals in FIGURES 2a and 2b indicate similar items or functions. A conventional switch mode power supply 400 of FIGURE 2b is coupled to a primary winding T1a of a chopper transformer T1. A secondary winding T1b is coupled to a half wave rectifier D1 and a filter capacitor C1 for generating a regulated supply voltage V20VP of +20V, in a conventional manner. Winding T1b is also coupled to a half wave rectifier D2 and a filter capacitor C2 for generating a regulated supply voltage V20VN of -20V.

Voltage V20VP is applied via a pair of an inductor L1 and a capacitor C11 forming a low pass filter to an emitter of a power switch transistor Q1a via a current sensing resistor R1. Inductor L1 and capacitor C11 attenuate high frequency switching transients of switch mode power supply 400. Similarly, voltage V20VN is applied via a pair of an inductor L2 and a capacitor C12 forming a low pass filter to an emitter of a power switch transistor Q2a via a current sensing resistor R12. When conductive, transistor Q1a applies voltage V20VP to, for example, a filter capacitor C5 to develop an output voltage OUT+ of +18V at a positive supply input terminal 660a of convergence amplifier 660 of deflection system 100 of FIGURE 2a. Similarly, when transistor Q2a of FIGURE 2b is conductive, voltage V20VN is applied to a filter capacitor C8 to develop an output voltage OUT- of -18V at a negative supply input terminal of FIGURE 2a of convergence amplifier 660. On the other hand, when disabled, transistor Q1a of FIGURE 2b decouples transformer T1 or voltage V20VP from terminal 660a of FIGURE 2a. Similarly, when disabled, transistor Q2a of FIGURE 2b decouples transformer T1 or voltage V20VN from terminal 660b of FIGURE 2a. Transistor Q1a of FIGURE 2b is controlled via a transistor Q1b that are coupled in a Darlington configuration to form a switched Darlington transistor Q1. Similarly, transistor Q2a is controlled via a transistor Q2b that are coupled in a Darlington configuration to form a switched Darlington transistor Q2.

A pair of resistors R14 and R17 form a voltage divider for voltage V20VP. A pair of resistors R14 and R17 provide a discharge path to ground for capacitor C1, when switch mode power supply 400 is turned off. Resistors R17 and R14 provide a .7V reference voltage across resistor R17 that is developed at the base of a transistor U1A. The base of a transistor U1B is coupled to capacitor C9 to develop a base voltage in transistor U1B that is proportional to the average value of a supply or load current IP. A sense resistors R1 develops a voltage VR1 that is indicative of a magnitude of supply current IP.

Transistors U1A and U1B are packaged to assure electrical matching and temperature tracking to form a temperature compensated comparator. A collector current is produced in transistor U1B, when the base voltage of transistor U1B is smaller than a threshold voltage determined by a ratio of the values of resistors R21 and R15 and voltage V20VP.

Voltage VR1 is low pass filtered in a filter that includes a resistor R2 and capacitor C9 for developing the base voltage of transistor U1B. The time constant of resistor R2 and capacitor C9 is selected for preventing short term or transient

overload such as an initial charging of output filter capacitor C5, during start-up, from falsely triggering the comparator formed by transistors U1A and U1B. Such false triggering of the comparator formed by transistors U1A and U1B could cause an undesired power supply shut down, during a short term or transient overload.

A similar arrangement is coupled to voltage V20VN and performs a similar function. Thus, a pair of NPN transistors U2A and U2B is analogous to the pair of PNP transistors U1A and U1B, respectively. A pair of resistors R15 and R21 is analogous to the pair of resistors R14 and R17, respectively. A resistor R12 is analogous to resistor R1. A resistor R11 and capacitor C6 are analogous to resistor R2 and capacitor C9, respectively.

A latch 60 that is controlled by the collector current in each of transistor U1B and U2B is formed by a pair of cross-coupled transistors Q4 and Q5. The base of transistor Q4 is coupled to the collector of transistor Q5 and the base of transistor Q5 is coupled to the collector of transistor Q4. An emitter of transistor Q5 is coupled via an emitter resistor to the base of transistor Q1b and to a series arrangement of a resistor R8 and a zener diode D3. A junction terminal 61 between inductor L1 and resistor R1 that develops a voltage level approximately equal to voltage V20P is coupled via an emitter resistor R19 to the emitter of transistor Q4 and via a collector resistor R5 to the collector of transistor Q5 and to the base of transistor Q4.

When the average value of each of current IP and current IN is normal or non-excessive, neither of voltage VR1 and VR12 is sufficient to turn on any of transistors U1B and U2B. Consequently, no collector current in produced in any of transistors U1B and U2B. Therefore, transistors Q4 and Q5 are turned off and remain in that state unless a fault condition occurs that causes any of current IP and current IN becomes excessive.

In the absence of a fault condition, no collector current is produced in either transistor U1B or U2B. Therefore, latch 60 is not triggered and transistors Q4 and Q5 are maintained turned off. The result is that the base current of transistor Q1 flows through resistor R8 and diode D3 causing base voltage 60a to be at a sufficiently low level to maintain transistor Q1a in saturation. As a consequence of transistor Q1a being in saturation, voltage OUT+ is developed at a normal operation level. At start up, transistor Q1 will turn on when the voltage V20VP rises to about 14 volts. Voltage 60a is also developed in a capacitor C10 that is coupled to the base of transistor Q1b. After transistor Q1 turns on, its collector voltage OUT+ rises to near +18V.

In carrying out an inventive feature, voltage OUT+ is coupled via a zener diode D4 and a resistor R9 to the base of Darlington transistor Q2. Transistor Q2a will turn on and be

in saturation when the difference between voltage OUT+ and voltage V20VN in capacitor C2, that reaches -20V, exceeds about 29V. At this voltage level, base bias current for transistor Q2 starts to flow in diode D4 and resistor R9. Consequently voltage OUT- is maintained at a normal operation level of -18V. By using voltage OUT+ to control the turn on of transistor Q2, a requirement, discussed before with respect to the power amplifier of the Rodriguez-Cavazos patent, that positive voltage OUT+ be developed before negative voltage OUT- is developed, is met.

When, as a result of fault, the average value of current IP in a current path that includes transistor Q1a or current IN in a current path that includes transistor Q2a is excessive, voltage VR1 or VR12 at a level that is sufficient to turn on transistor: U1B or U2B, respectively, appears across filter capacitor C9 or C6. Consequently, the collector current in transistor U1B or U2B, that is coupled via a resistor R3 or a resistor R7 to the base of transistor Q5 or Q4, respectively, will trigger latch 60. Resistor R19 and a resistor R10 limit a transient current that results from the rapid discharge of capacitor C10, during the transition of latch 60 to operation in a latching mode.

The latching mode in latch 60 is maintained by a current flowing from terminal 61 and produced by voltage V20VP through transistors Q4 and Q5, resistor R8 and diode D3. The action of transistor Q4 and Q5 is similar to that of a silicon controlled switch (SCS). Transistors Q4 and Q5 are used to achieve a low sustaining current and a low cost. A silicon controlled rectifier (SCR) cannot be conveniently used because the collector currents in transistors U1B and U2B that are required to trigger latch 60 are at opposite polarities. The saturation voltage across transistors Q4 and Q5 is about .7V.

The switching state of Darlington transistors Q1 and Q2 are controlled by an output voltage 60a of latch 60. Transistors Q4 and Q5, when latch 60 operates in the latching mode, shunt the base emitter of Darlington transistor Q1. Therefore, a collector current in transistor Q5 increases the base voltage of transistor Q1b in a manner to turn off transistor Q1a. Thus, transformer T1 is decoupled from amplifier 660 of FIGURE 2a. Consequently, voltage OUT+ is disabled.

A secondary winding T1c of transformer T1 of FIGURE 2b is coupled to a diode 19 for generating a supply voltage VPS1 that energizes stages of the television receiver, for example, output stage 600 of FIGURE 2a. When voltage OUT+ of FIGURE 2b and voltage OUT- are disabled , as a result of a fault, as explained before, output stage 600 of FIGURE 2a remains, advantageously, operational. This facilitates service operation. Thus, transformer T1 forms a common power stage for both output stage 600 and amplifier 660 of FIGURE 2a.

During a transient overload condition such as, during start-up, when filter capacitors C5 and C6 of FIGURE 2b are charged, current IP in transistor Q1 or current IN is limited by a zener diode D5 and a zener diode D6, respectively, so that the maximum current ratings of Darlington transistors Q1 and Q2 are not exceeded. Zener diode D5, for example, is coupled between terminal 61 and the base of transistor Q1b.

Capacitors across the base emitter-base terminals of the various transistors prevent turn on of the transistors by induced radio frequency currents. Capacitors across the various zener diodes prevent radio frequency radiation.

20040407.0037

Abstract Of The Disclosure

In a projection television receiver, a common switch mode power supply energizes the convergence circuits and the rest of the circuits of the projection television receiver. In normal operation, a switch couples a supply voltage produces in the common switch mode power supply to the convergence circuits. When, as a result of a fault, a supply current in the convergence circuits is excessive, the common switch mode power supply is decoupled from the convergence circuits for disabling the current in the convergence circuits. Thus, the rest of the circuits in projection television receiver remain energized and operative.

EL912754351US

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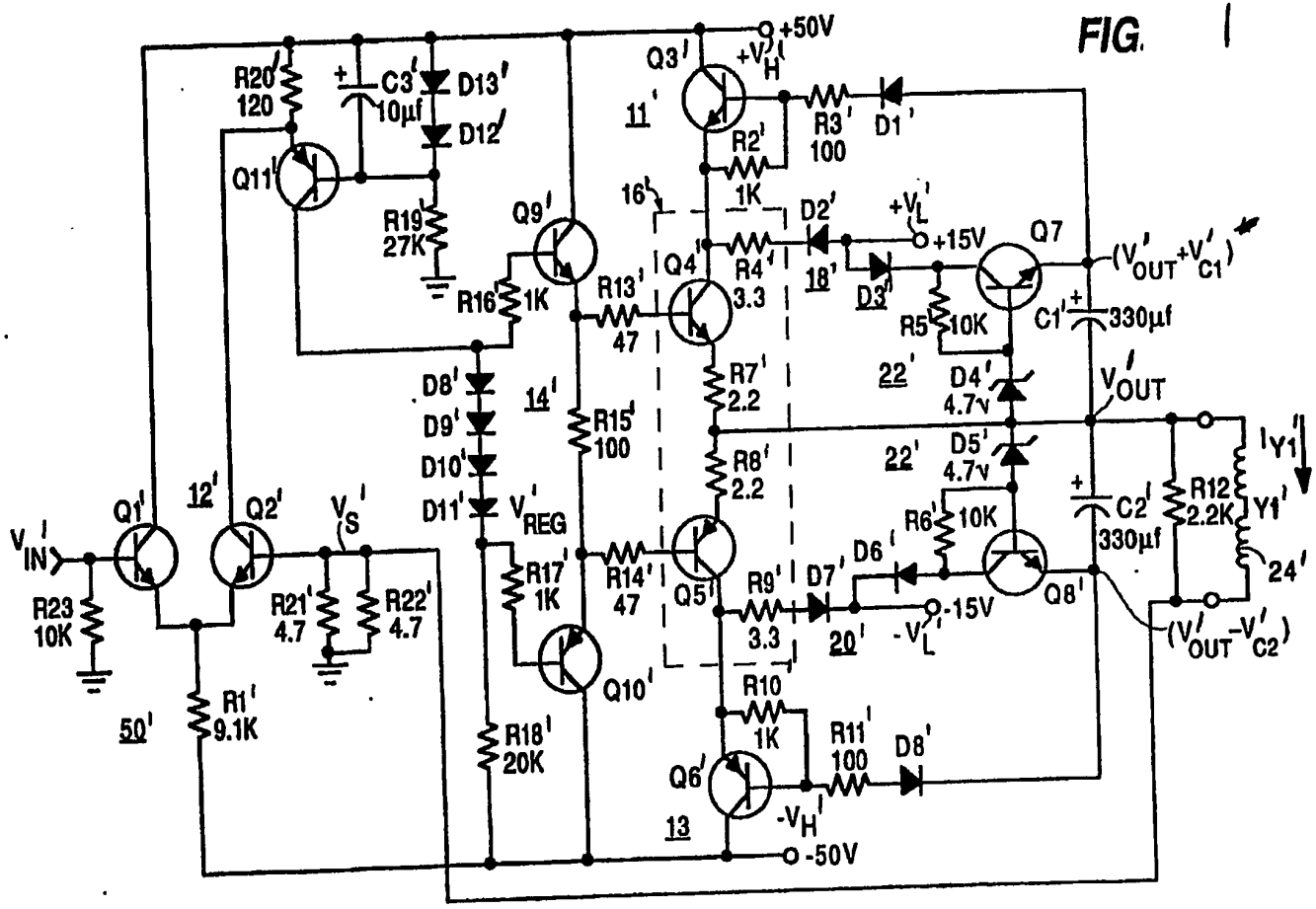
FIG. 1



PRIOR ART

20h0h0 T200ZE09

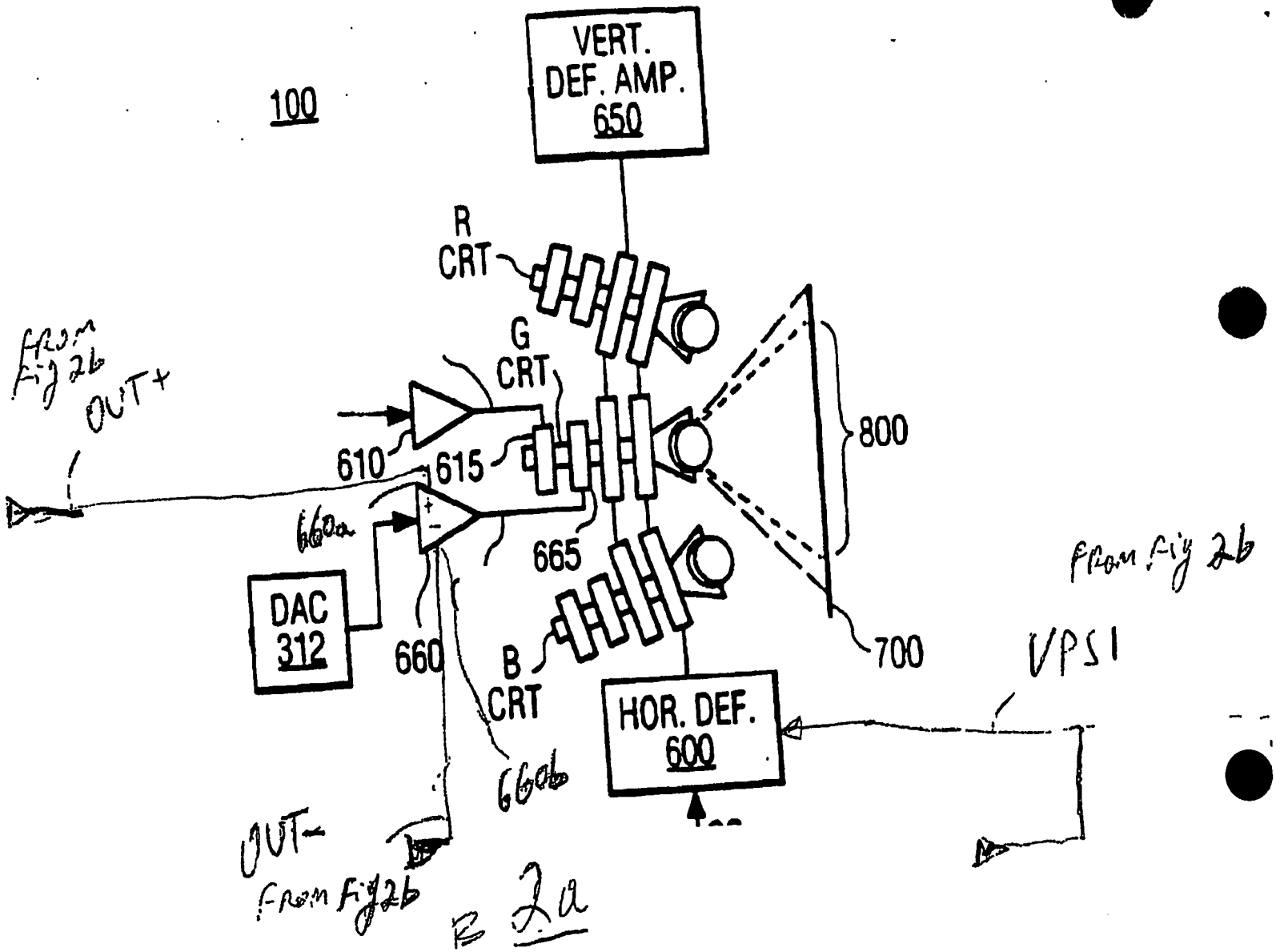


FIG 2a

20040810 1700260